

### Features

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

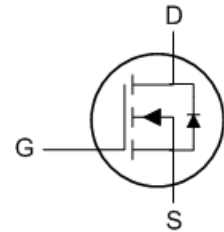
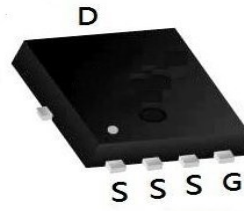
- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

### Product Summary



BVDSS	RDSON	ID
100V	4.5mΩ	100A

### PDFN5X6 Pin Configuration



### Absolute Maximum Ratings ( $T_c = 25^\circ\text{C}$ , unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_c=25^\circ\text{C}$	$I_D$	100	A
	$T_c=100^\circ\text{C}$		60	
Pulsed Drain Current <sup>4</sup>		$I_{DM}$	380	A
Single Pulse Avalanche Energy <sup>3</sup>		<b>EAS</b>	205	mJ
Total Power Dissipation	$T_c=25^\circ\text{C}$	$P_D$	113.6	W
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient <sup>1</sup>	$R_{\theta JA}$	58	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.1	$^\circ\text{C/W}$

**N-Ch100V Fast Switching MOSFETs**
**Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise noted)**

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	100	-	-	V	
Gate-body Leakage current	I <sub>gss</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V	T <sub>J</sub> = 25°C	-	-	1	μA
			T <sub>J</sub> = 100°C	-	-	100	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1.2	1.8	2.5	V	
Drain-Source on-Resistance <sup>2</sup>	R <sub>DSON</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	4.5	6	mΩ	
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 15A	-	6.6	9		
<b>Dynamic Characteristics</b>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, f = 1MHz	-	4400	-	pF	
Output Capacitance	C <sub>oss</sub>		-	645	-		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	20	-		
<b>Switching Characteristics</b>							
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz	-	1.7	-	Ω	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 50V, I <sub>D</sub> = 20A	-	75	-	nC	
Gate-Source Charge	Q <sub>gs</sub>		-	17	-		
Gate-Drain Charge	Q <sub>gd</sub>		-	13	-		
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 50V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	15.4	-	ns	
Rise Time	t <sub>r</sub>		-	13	-		
Turn-off Delay Time	t <sub>d(off)</sub>		-	34	-		
Fall Time	t <sub>f</sub>		-	6.2	-		
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>2</sup>	V <sub>SD</sub>	I <sub>F</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V	
Continuous Source Current <sup>1,5</sup>	I <sub>S</sub>	V <sub>G</sub> = V <sub>D</sub> = 0V, Force Current	-	-	95	A	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20A, dI/dt = 100A/μs	-	55	-	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	101	-	nC	

**Notes:**

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C.
2. The EAS data shows Max. rating. The test condition is V<sub>DD</sub> = 25V, V<sub>GS</sub> = 10V, L = 0.4mH, I<sub>AS</sub> = 40A
3. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.

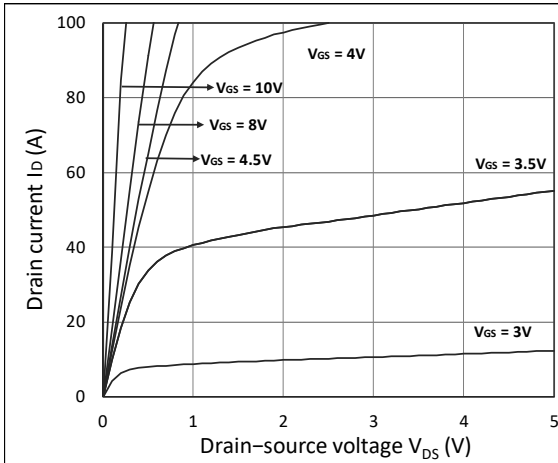
**Typical Characteristics**


Figure 1. Output Characteristics

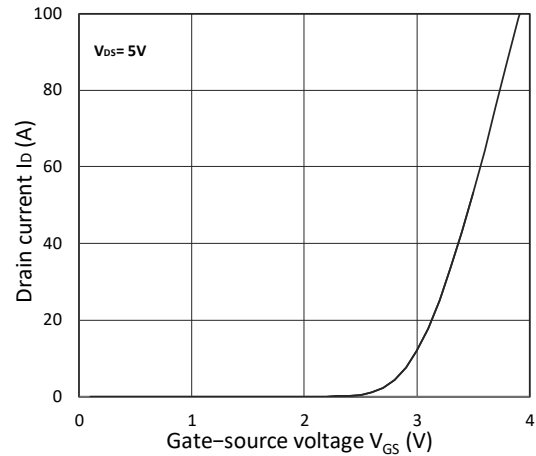


Figure 2. Transfer Characteristics

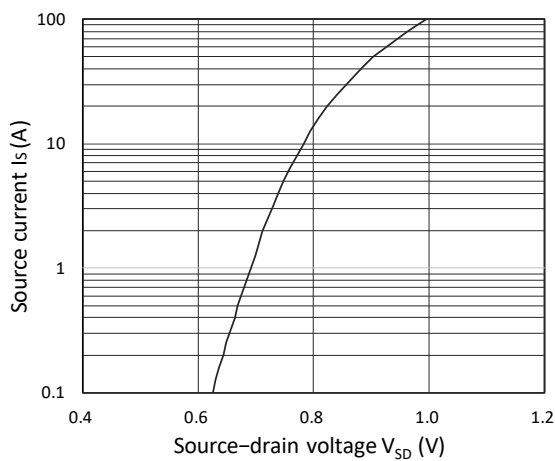
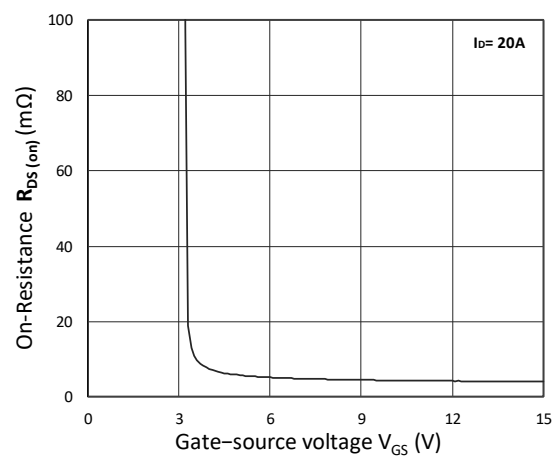
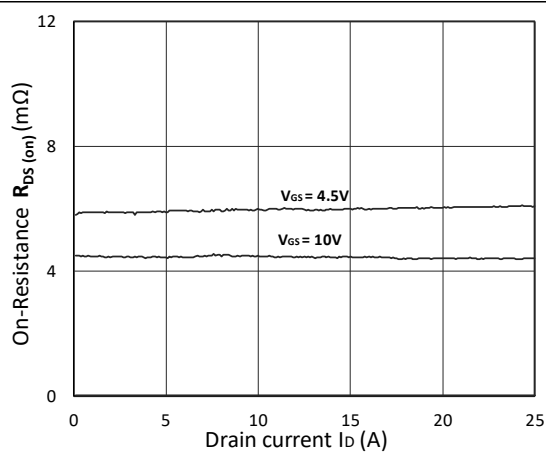
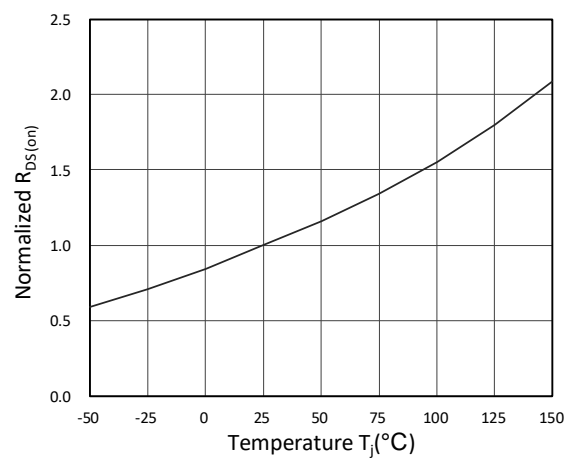


Figure 3. Forward Characteristics of Reverse


 Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$ 

 Figure 5.  $R_{DS(on)}$  vs.  $I_D$ 

 Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

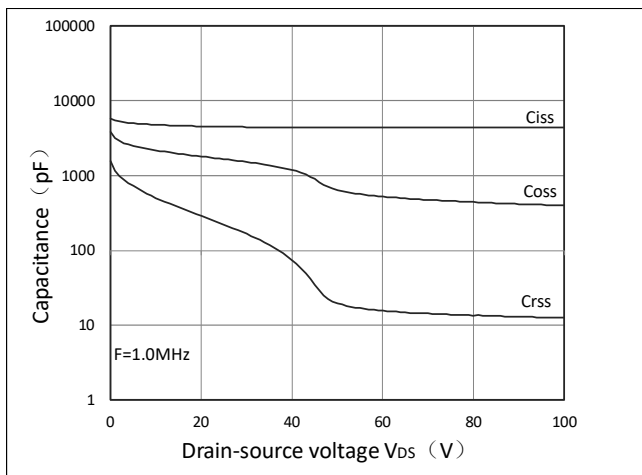


Figure 7. Capacitance Characteristics

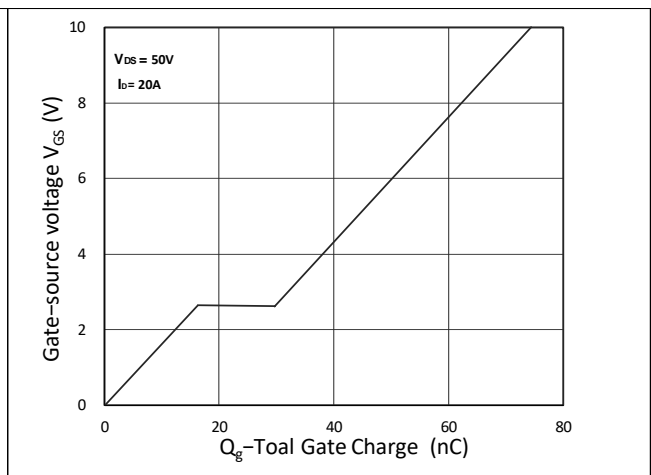


Figure 8. Gate Charge Characteristics

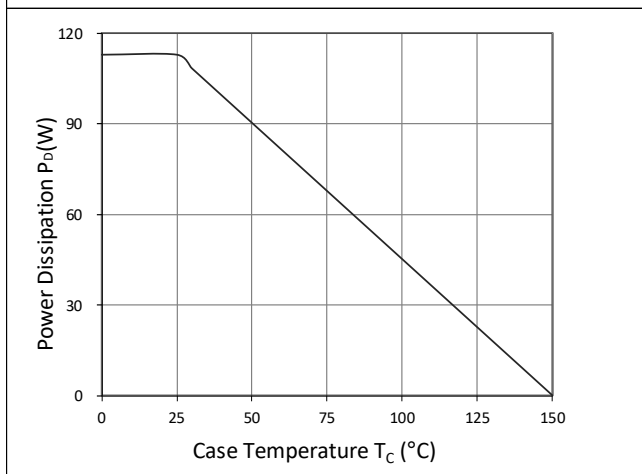


Figure 9. Power Dissipation

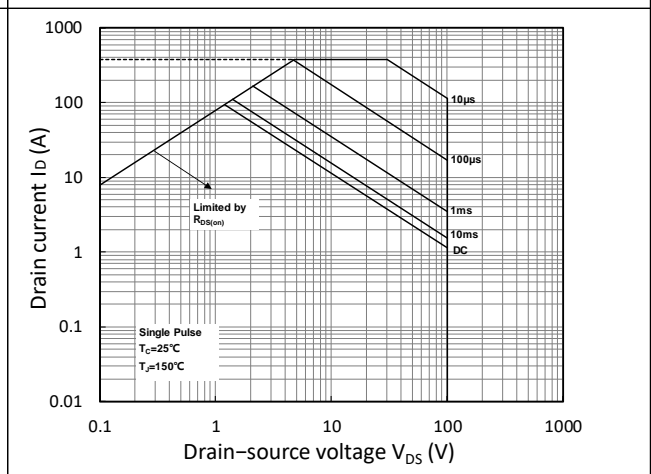


Figure 10. Safe Operating Area

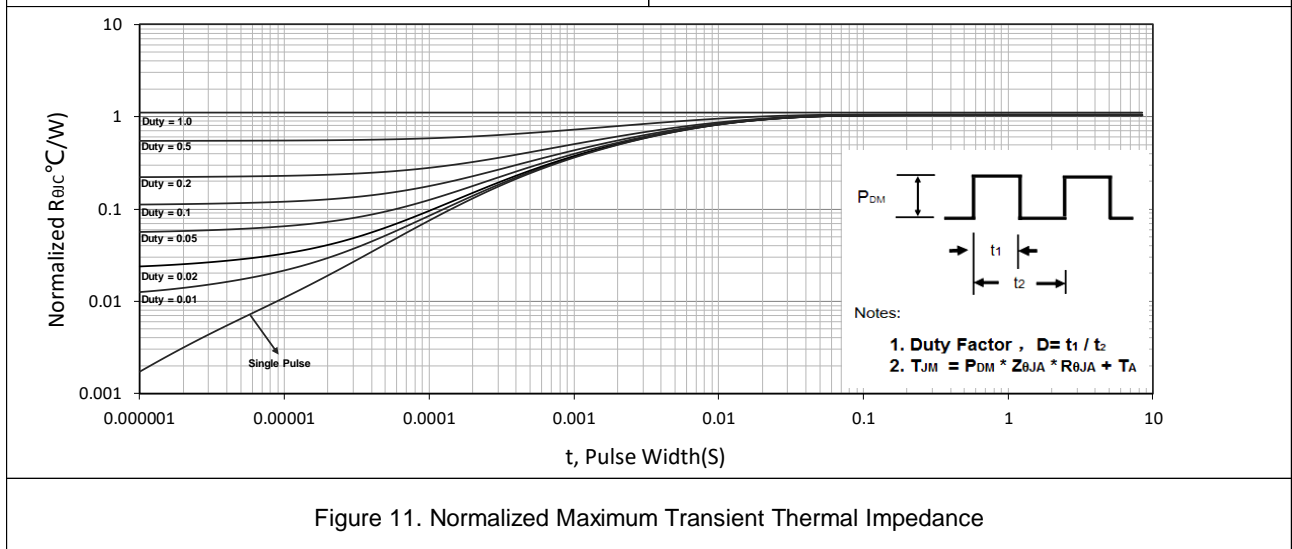


Figure 11. Normalized Maximum Transient Thermal Impedance

■ Test circuits and waveforms

N-Ch100V Fast Switching MOSFETs

Test Circuit

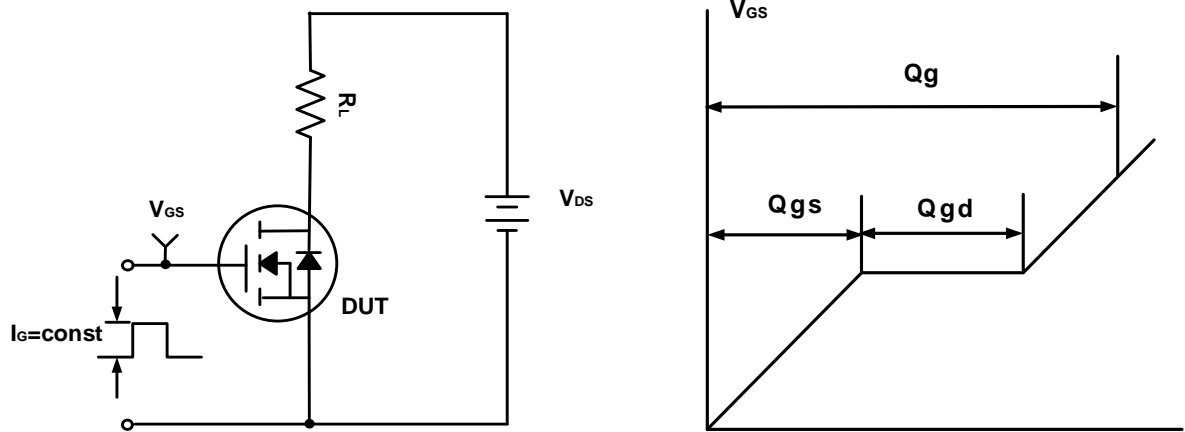


Figure A. Gate Charge Test Circuit & Waveforms

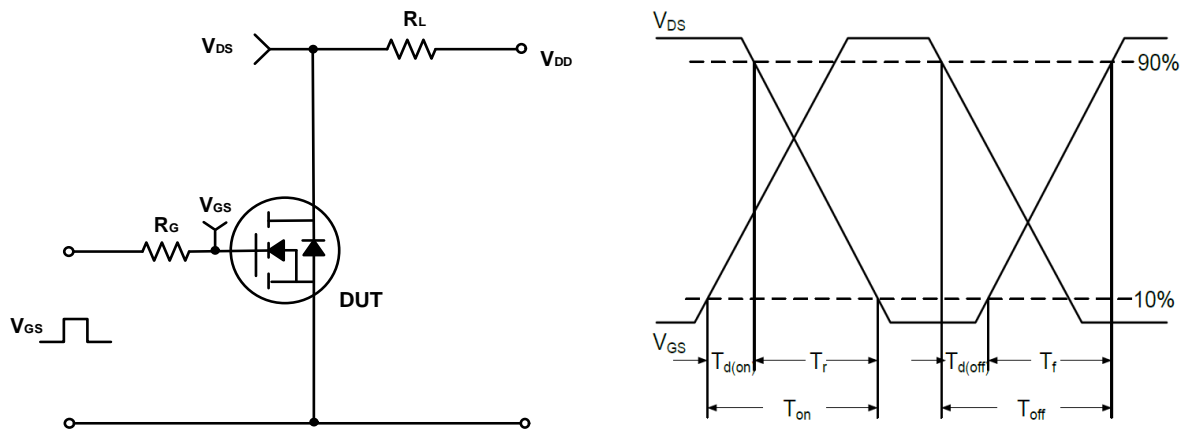


Figure B. Switching Test Circuit & Waveforms

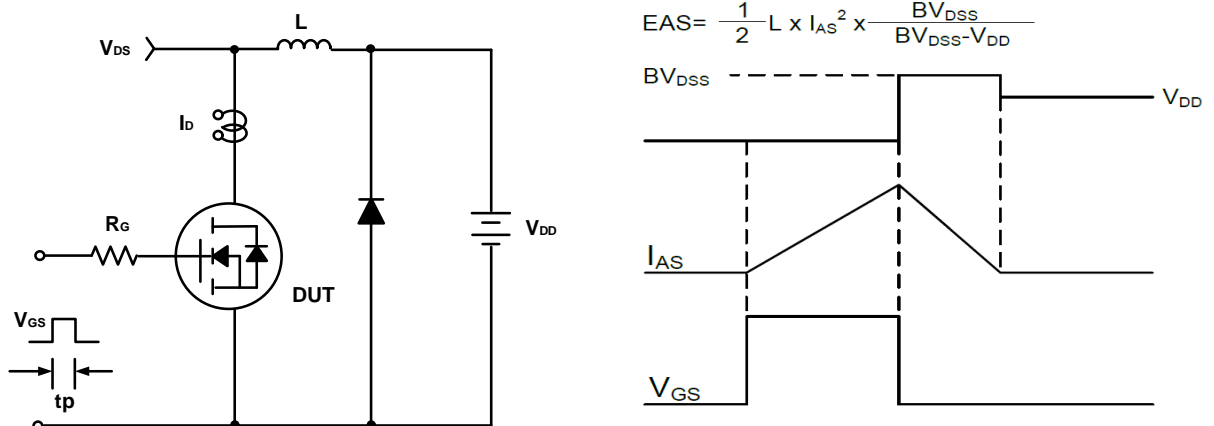
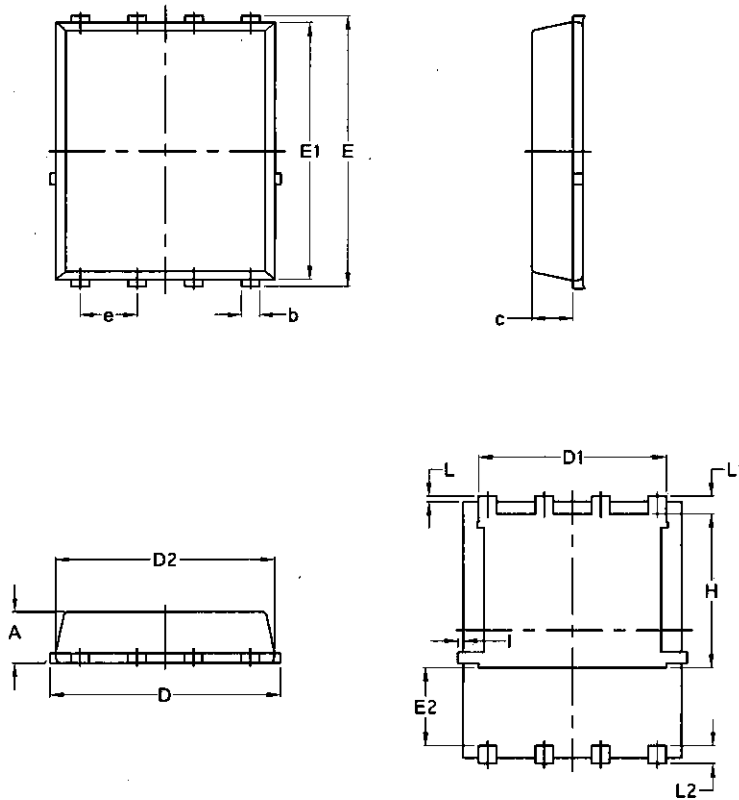


Figure C. Unclamped Inductive Switching Circuit & Waveforms

**Package Mechanical Data-DFN5\*6-8L-Single**


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070